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Customer No. 31561
Docket No. 12978-US-PA
Application No.: 10/710,420

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Applicant : Wu et al.
 Application No. : 10/710,420
 Filed : July 9, 2004
 For : METHOD FOR REDUCING STANDARD DELAY
 FORMAT FILE SIZE
 Examiner : MEMULA, SURESH
 Art Unit : 2825

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In response to the Notice of Appeal filed on November 1, 2006, please find the relevant paper as follows:

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Please charge the payment in the amount of US\$500 to Account No. 50-2620 (Order No.:12978-US-PA) to cover the fee set forth in 37 CFR 1.17(c) for filing the Appeal Brief.

If the payment is not fully covered in response thereof, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No.: 50-2620 (Order No.:12978-US-PA).

Thank you for your attention and assistance in this matter. If you have any questions, please feel free to contact the undersigned.

Respectfully Submitted,
 JIANQ CHYUN Intellectual Property Office

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE Wu et al.

Application for Patent

Filed: July 9, 2004

Serial No. 10/710,420

FOR:

**METHOD FOR REDUCING STANDARD DELAY FORMAT
FILE SIZE**

(as amended)

APPEAL BRIEF

JIANQ CHYUN Intellectual Property Office
Representative for Applicants

Attorney Docket No. 12978-US-PA

USSN 10/710,420

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Appeal Brief

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PATENT**I. Real party in interest**

The real party in interest is Faraday Technology Corp., the assignee of record.

II. Related appeals and interferences

There are no related appeals and/or interferences.

III. Status of the claims

A total of 5 claims were presented during prosecution of this application. The Appellants appeal the rejected claims 1-5.

IV. Status of amendments

A proposed amendment was filed by Appellants on 10 May 2006, proposing amendments to claims 1-5 in response to the rejection under 35 U.S.C. 112 in the 1st Office Action dated on 8 March 2006. Another proposed amendment was filed by Appellants on 30 August 2006, proposing amendments to the specification, the abstract, claim 1 and claim 3 of the application in response to the objection in the Final Office Action dated on 5 June 2006. All the proposed amendments have been admitted to enter by the Examiner.

V. Summary of claimed subject matter

The claimed subject matter of the present invention involved in the appeal is directed to a method for reducing an SDF file size. The method is configured to remove the state-dependent descriptions, which are not intended to be used, from the cell descriptions of the original SDF file 220 such as IEEE 1497 SDF file, by referring to a design description 210, such as, a netlist, so as to generate a reduced size SDF file 240 such that the simulation result generated by a simulator is not affected with the reduced SDF file.

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For a cell with more than two I/O paths, it is common that the cell description of the SDF file contains a state-dependent description. The so-called state-dependent description herein indicates that a delay data of the I/O path is described by a description associated to different input status of the cell. As taught in paragraph [0020], if it is determined that the state-dependent description is present in the cell description, the process proceeds to step 340, where the state-dependent descriptions in the cell description, which are not intended to be used, are removed by referring to a state data which is present in the IC design description and is associated to the cell description, so as to reduce the SDF file size.

VI. Grounds of rejection to be reviewed on appeal

Were claims 1-4 properly rejected under 35 U.S.C. 102(b) as being anticipated by Rich et al. (US Pub. 2003/0125917)?

Was claim 5 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Rich et al. in view of Rupp et al. (US 6,857,110)?

VII. Arguments

A. The related laws

In order to properly anticipate Applicants' claimed invention under 35 U.S.C. § 102(b), each and every element of the claim in issue must be found "either expressly or inherently described, in a single prior art reference." "The identical invention must be shown as complete detail as is contained in the ... claim" *Richardson v. Suzuki Motor Co.*, 868 F. 2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). See M.P.E.P. § 2131, 8th ed., 2001.

The standard for lack of novelty is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1986).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

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For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. These elements must be arranged as in the claim under review. *In re Bond*, 910, F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The inquiry as to anticipation is symmetrical with the inquiry as to infringement of a patent. A classic test of anticipation provides : That which will infringe, if later, will anticipate, if earlier. *Knapp v. Morss*, 150 U.S. 221, 37 L. Ed. 1059, 14 S. Ct. 81 (1893); *Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1459, 221 U.S.P.Q. 481 (Fed. Cir. 1984). Therefore, by analogy, the all elements rule used for a determination of infringement finds its applicability in a determination of anticipation. Discussion of the all elements rule can be found in *Becton Dickinson and Co. v. C.R. Bard Inc.*, 17 U.S.P.Q. 2d 1962, 1967 (Fed. Cir 1989) and *Hi-Life Products Inc. v. American National Water-Mattress Corp.*, 6 U.S.P.Q.2d 1132, 1133 (Fed. Cir. 1988).

To establish a prima facie case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." MPEP § 2143, 8th ed., February 2003.

A claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C § 103(a); see *Graham v. John Deere Co.*, 383 U.S. 1, 14, 86 S. Ct. 684, 15 L.Ed.2d 545, 148 USPQ 459, 465 (1966).

"The inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." *Hartness*

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International, Inc. Vs. Simplimatic Engineering Co., 819 F2d 1100, 1108, 2 USPQ 2D 1826 (Fed. Cir. 1987).

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

"Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blue print for piecing together the prior art to defeat patentability—the essence of hindsight". *In re Dembicza*k, 175 F.3d at 999.

"It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements from the references to fill the gaps". *In re Gorman*, 933 F.2d 982, 987, 18 USPQ 2d 1885 (Fed. Cir. 1991).

B. Grouping of the claims

For the first ground of rejection contested by Appellants in this appeal, claims 1-4 may be treated as one group, and independent claim 1 may be taken as the representative for the issue on appeal. For the second ground of rejection contested by Appellants in this appeal, claim 5 may be treated as another group, and claim 5 may be taken as the representative for the issue on appeal.

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C. *Claims 1-4 were improperly rejected under 35 U.S.C. 102(b) as being anticipated by Rich et al. (US Pub. 2003/0125917)*

1. The rejection

Claims 1-4 were improperly rejected under 35 U.S.C. 102(b) as being anticipated by Rich et al. (US Pub. 2003/0125917) in the Office Action mailed on 3/8/2006, and such rejections were further improperly maintained in the Final Office Action mailed on 6/5/2006, and in the Advisory Action mailed on 9/26/2006, respectively.

In making the rejection, the Examiner indicated "Paragraphs 0008, 0043, and FIGS. 2, 4-6, 10, and 14" as evidence of Rich et al. having taught a method comprising a step of "determining whether or not a state-dependent description is present in the cell description". The Examiner also indicated that "Paragraphs 0035, 0036, 0037, 0043, 0093, 0100 and FIGS. 1-2, 4-6, and 22" as evidences of Rich et al. having taught a step of "removing the state-dependent description in the cell description, which are impossible to be used, by referring to a state data contained in a design description and associated to the cell description when it is determined that the state-dependent description is present in the cell description".

In replying Appellants' arguments, the Examiner answered in the Final Office Action dated 06/05/2006:

"First, Paragraph 0007 in the instant application states: 'the delay data of each I/O path contains four state-dependent descriptions', which corresponds to one or more of 'delay entries', 'delay values', and 'delay data' in Rich.

Secondly, in accordance with the above, the SDF file size is reduced by removing state-dependent descriptions. Note that although the exact phraseology 'which are impossible to be used' is not recited in Rich, one or more of the following corresponds to the 'impossible to be used' limitation in claim 1:

- A. To avoid a 'size penalty'
- B. Duplicated delay is impossible to be used, i.e., redundancy
- C. '.. to complete a simulation in a timely manner'

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D. "...the SDF analysis file, allows for certain portions of the SDF to remain untouched, for robustness"; i.e., why remove portions that could possibly be used or are essential".

2. The prior art

The prior art reference of Rich et al. select delay values from a VHDL standard delay file that corresponds to an instance of a logic gate in a logic model. Then the system collects all the delay values of the selected instance and builds super generics for the rise-time and the fall-time of the selected instance. Then, the system repeats this process for every delay value in the standard delay file that corresponds to every instance of every logic gate in the logic model. The system then outputs a reduced size standard delay file containing the super generics for every instance of every logic gate in the logic model. According to Rich's paragraph 100, Rich can reduce SDF file size because each super generic is represented by a collection of pointers into a data structure containing all the relevant delay values. For each instance, the collection of pointers, that point into the data structure for the super generic to be able to resolve the actual delay values for the particular instance, takes up significantly much less storage than a set of conventional generics.

The only removal performed by Rich is at step 607 in Fig. 6. According to paragraph 54 of Rich, all the delays assigned to a generic for the entire chip are extracted from the values in the SDF file. The delays are sorted and any duplicate delay entries are removed. Then the sorted delays are grouped into sets of up to 62 entries corresponding to correlation sets.

3. The prior art differentiated

Appellants disagree with the Examiner's reasoning.

Claim 1 reduces SDF file sizes by removing state-dependent descriptions which are not intended to be used. According to paragraphs 18 and 19 of the specification of the instant application, the state-dependent descriptions removed in claim 1 are descriptions associated with the states which will not appear during normal operation conditions of an IC. The states of a cell are the logic 0/1 combinations of the input terminals of the cell.

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Appellants submit that Rich et al. fail to teach the step of "determining whether or not a state-dependent description is present in the cell description" in claim 1. Rich does not even teach state-dependent descriptions. As mentioned above, state-dependent descriptions are delay descriptions associated with the logic states of input terminals of a cell. Although Rich discloses logic gates with multiple input terminals, Rich does not consider logic state combinations of the input terminals of each cell. In other words, Rich et al. neither teaches nor suggests the concept of state dependency of claim 1. As a result, Rich et al. neither teaches nor suggests any action performed on state-dependent descriptions, including "determining whether or not a state-dependent description is present in the cell description". It is unfair for the Examiner to ignore such a fact.

Appellants also submit that Rich et al. fail to teach the step of "removing the state-dependent descriptions in the cell description, which are not intended to be used, by referring to a state data contained in a design description associated to the cell description when it is determined that the state-dependent description is present in the cell description" in claim 1. Since Rich does not teach the concept of state as recited in claim 1, it is impossible for Rich to teach the "state data contained in the design description". It is also impossible for Rich to teach "state-dependent descriptions which are not intended to be used". And Rich's approach does not make decisions based on whether "the state-dependent description is present in the cell description".

Rich removes only duplicate delay entries, which are absolutely different from the state-dependent descriptions removed in claim 1. State-dependent descriptions not intended to be used do not have to be duplicate, since they may appear only once in an SDF file. From another point of view, duplicate delay entries may all be used by the simulator because they may belong to different gate instances on frequently used transmission paths. Rich teaches nothing about the possibility of delay entries to be used. Rich simply removes and correlate delay entries regardless of their state dependency and possibility to be used. It is unfair for the Examiner to ignore such differences.

In response to Appellants' remarks, the Final Office Action dated on 5 June 2006 stated that paragraph 7 of the application states: "the delay data of each I/O path contains four state-dependent descriptions", which corresponds to one or more of "delay entries", "delay values", and "delay data" in Rich. Appellants respectfully disagree. For reasons shown

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above, the generic delay entries in Rich cannot be equated with the state-dependent delay descriptions in claim 1.

In response to Appellants' remarks, the Final Office Action enumerated four features (A-D) in Rich corresponding to the "impossible to be used" (now "not intended to be used") limitation in claim 1. Appellants respectfully disagree. The reasons are listed below.

In regard to features A and C, although claim 1 and Rich have similar purposes, that is, reducing SDF file sizes, the conclusion that the limitations of claim 1 are disclosed by Rich should not be reached through hindsight merely because claim 1 and Rich have similar purposes. As mentioned above, the steps taken by claim 1 and Rich to reduce SDF file sizes are patently distinguishable. Rich et al. removes duplicate delay entries, whereas claim 1 removes state-dependent descriptions not intended to be used. The duplicate delay entries in Rich et al. are in no way analogous to the state-dependent descriptions in claim 1.

In regard to feature B, "duplicated delay is impossible to be used, i.e., redundancy", the duplicate entries in Rich is not equivalent to the delay descriptions removed in claim 1. Claim 1 removes redundant state-dependent delay descriptions, which have to be determined by referring to the design description of the IC (paragraphs 18 and 19). In comparison, Rich teaches neither input state nor state dependency.

In regard to feature D, Appellants believes that it is irrelevant to the anticipation of claim 1 by Rich et al.

Accordingly, Appellants submit that "the impossible to be used" that is later amended to be "not intended to be used" limitation is not at all anticipated by Rich et al. The duplicate delay entries disclosed in Rich et al. were improperly interpreted in the Final Office Action to be analogous to the state-dependent descriptions not intended to be used in claim 1.

Based on the differences shown above, claim 1 of the instant application is patently distinguishable from Rich et al.

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D. *Claim 5 was improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Rich et al. in view of Rupp et al.*

1. The rejection

Claim 5 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Rich et al. (US Pub. 2003/0125917) in view of Rupp (US Patent 6,857,110) et al. in the Office Action mailed on 3/8/2006, and this rejection was further improperly maintained in the Final Office Action mailed on 6/5/2006, and in the Advisory Action mailed on 9/26/2006, respectively.

2. The prior art

As stated above, Rich et al. reduces SDF file size by removing duplicate delay entries.

Rupp et al. teaches the SDF IEEE 1497 file in claim 5.

3. The prior art differentiated

Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Rich et al. in view of Rupp et al. Appellants disagree with the Examiner's reasoning and submit that as traversed above, claim 5 depends on allowable base claim 1, and thus is also allowable.

4. Even if combined Rich et al. and Rupp et al.

As submitted by Appellants above, Rich does not teach all limitations of claim 1. Claim 5 depends on claim 1 and includes all limitations of claim 1. Therefore, adding Rupp's SDF IEEE 1497 file into Rich does not help to render claim 5 obvious. Claim 5 is patentable over the combination of Rich et al. and Rupp et al.

E. Conclusion

As noted, the Examiner has not properly applied 35 U.S.C. § 102 and U.S.C. § 103 in his rejections of the claims at issue. Accordingly, Applicants believe that the rejections

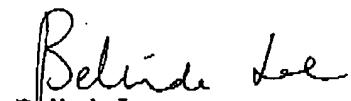
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under 35 U.S.C. § 102 and U.S.C. § 103 to be improper, and respectfully request the Board of Appeals and interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully submitted,

Date : Dec. 27, 2006


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VIII. Claims appendix

CLAIMS ON APPEAL:

1. (previously presented) A method of reducing an SDF file size, comprising:
reading a cell description from the SDF file;
determining whether or not a state-dependent description is present in the cell
description; and

removing the state-dependent descriptions in the cell description, which are not
intended to be used, by referring to a state data contained in a design description associated to
the cell description when it is determined that the state-dependent description is present in the
cell description.

2. (previously presented) The method of reducing the SDF file size of claim 1,
wherein when the state-dependent description is not present in the cell description, the cell
description is kept unchanged in the SDF file.

3. (previously presented) The method of reducing the SDF file size of claim 1,
wherein when the state-dependent description is present in the cell description and there is no
delay data description associated to the state, which is not intended to be used, the cell
description is kept unchanged in the SDF file.

4. (previously presented) The method of reducing the SDF file size of claim 1,
wherein the design description is a netlist.

5. (previously presented) The method for reducing the SDF file size of claim 1,
wherein the SDF file is an IEEE 1497 SDF file.

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IX. Evidence appendix

There is no evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the examiner.

X. Related proceedings appendix

There are no decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief.